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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 02998.P011 Total Pages 2

First Named Inventor or Application Identifier Wingard, et al.

Express Mail Label No. EL234218166US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 13)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 8)

4. X Oath or Declaration (Total Pages 6)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. X Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __ Other: ____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
____ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _

18. **Correspondence Address**
____ Customer Number or Bar Code Label _____
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or
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Attorney Docket: 02998.P011 *PATENT*

UNITED STATES PATENT APPLICATION

FOR

LOGIC SYSTEM WITH CONFIGURABLE INTERFACE

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LOGIC SYSTEM WITH CONFIGURABLE INTERFACE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a configurable interface enabling straightforward re-use of a core with different interfaces.

2. Art Background

The latest advances in semiconductor technology and design methodology have enabled the emerging market for System-On-a-Chip (SoC) designs. Full systems, consisting of more than several million logic gates, can now be implemented in a single chip. One of the main design challenges in these SoC designs is the logical and physical interconnect that allows communication between the subsystem cores that compose the design. These cores typically fall into different categories: computing cores such as a CPU (central processing unit), DSP (digital signal processor) or floating point co-processor; peripheral interface cores such as PCI (personal computer interface) or USB (universal serial bus); memory blocks such as SRAM (static random access memory) and on-chip DRAM (dynamic random access memory); and application specific blocks such as video cores (MPEG-motion pictures experts group) or communication cores.

Since many of the SoC designs are targeted towards communications and consumer applications, time-to-market is a critical factor in the decision process on the level of integration to be used in a particular product. Once a core has been proven in one design, it becomes very attractive to re-use the core in later designs. While choosing a proven design may eliminate the time that would otherwise be required to design a new core, design re-use offers the promise of many other benefits. First, a model may be written for the proven core that can provide accurate results when analyzing the requirements and performance of a

new system design; the model for a new, unproven core is likely to be neither as accurate as the proven core, nor built in time to influence the design. Second, proven cores can serve as building blocks that simplify the overall design process by allowing the system designer to focus at a higher level of abstraction, while providing improved predictability in the resulting system implementation. Third, re-use of hardware cores protects the investment in software to control those cores, and allows the system software implementation to proceed as soon as the hardware building blocks have been chosen. Finally, core re-use protects the investment in verification and testing. Since the desired systems are highly integrated, the required cores end up deeply embedded within an integrated circuit. In deeply-embedded designs, verifying the design functionality becomes very challenging and testing an individual system to prove that it is correctly built can lead to expensive delays or costly system rework. Thus, maintaining the integrity of core verification and testing is likely the single biggest gain from design re-use.

However, historically, re-using cores has not been efficient. One of the challenges in the re-use of these cores is that, dependent on the system requirements of the SoC that the core is used in, different performance levels and features are required from the core. Moreover, many applications of SoC are targeted towards consumer applications where providing the most cost-effective solution is very important.

The interface of the core has been a source of inefficiency in core re-use. **Figure 1a** shows a representation of a core with a particular interface. Inefficiencies arise when this core must be re-used in a different system that requires a different interface of the core, or demands different requirements of the core.

One option is to re-design the interface of the core. This solution may offer area and performance benefits, but is expensive in term of time, effort and design risk. The effort involved is not only in terms of design time but there is also

significant additional work in verification and validation. This solution is represented in **Figure 1b**, which shows the core with the optimized interface.

Rather than changing the core, some designers opt to leave the core as is, and adapt the system level interconnect to the existing core interface. While it preserves the integrity of the original core, it leads to many other inefficiencies. With respect to performance, the logic that integrates the core into the system can add latency into the system, which can adversely affect the system performance. With respect to cost, the additional logic can add a significant number of gates to the design and hence increase the chip area and hence the cost. This solution is represented in **Figure 1c**.

SUMMARY

The system and method of the present invention provides a core or subsystem with a configurable interface that enables straightforward re-use of the core. In one embodiment, code representative of the core and configurable interface parameters are combined with input consisting of the defined configurable interface parameters to generate a core having an interface configured in accordance with the defined interface parameters.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will be apparent from the following detailed description in which:

Figure 1a, 1b, and 1c illustrate prior art techniques relating to core interfacing.

Figure 2a and 2b illustrate one embodiment of a logic interface.

Figure 3a, 3b, and 3c illustrate embodiments of configurable interface parameters.

Figure 4 illustrates one embodiment of an interface generated in accordance with the teachings of the present invention.

Figure 5 is an example of a configuration file.

Figure 6 illustrates one embodiment of a process for generating a core using a previously configured interface.

Figure 7 is an example of a graphical user interface utilized in one embodiment to select a configuration of the interface.

DETAILED DESCRIPTION

In the system and the method of the present invention, the above challenges of creating optimal cores for a particular system are resolved by implementing a core with a highly configurable interface, such that the core together with its interface can be optimally configured for the particular system that the core is used in. In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. In other instances, well-known electrical structures and circuits are shown in block diagram form in order not to obscure the present invention unnecessarily.

The system and the method of the present invention will be explained by example, initially referring to **Figure 2a**. **Figure 2a** shows exemplary signals of a simple logical interface. The signals include a request phase that includes command, address, data and command accept, and a response phase that includes response and data. **Figure 2b** illustrates an interface providing the connection between two cores. For purposes of discussion herein cores are defined as logic or circuitry that performs a function or functions that receives input and/or generates output at least in part through a configurable interface.

In one embodiment, the function to be performed can be specified by the MCmd lines of **Figure 2b**. One embodiment of the MCmd encoding specifies read, write and exclusive read functions, as shown in **Figure 3a**. Such functions may represent typical operations performed in computer systems. For instance the exclusive read may indicate that a read to a specific address must be followed by a write to the same address before any other core in the system can read that location.

In one embodiment, the command encoding can be as given in **Figure 3a**. The encoded functions are functions that are typically used in computer systems.

Exclusive Read indicates that a read to a specific address must be followed by a write to the same address before any other core in the system can write that location.

The above interface illustrated by **Figure 2a and 2b and 3a** is a simple interface and can be used when the core only needs to support low-performance requirements from the system. One can now extend the interface to incorporate additional functional and performance related features in a configurable manner such that the core support many different combinations on interface options. In alternate embodiments, fewer or additional types of configurability may be implemented. In one embodiment herein, there are three different types of configurability.

In an exemplary type of configuration, one can configure the width of a particular field. As an example, the width of the address field can be configured to be a value between 1 and 32 lines. This allows the core to be used in systems that require different sizes of address space. This type of configurability is referred to herein as "parametrization".

In an exemplary second type of configuration, one can select the availability of certain interface functions. In the command-encoding example of **Figure 3a**, one can make the function "Exclusive Read" a configurable option, such that this function can be enabled when the core is used in a system that requires this. This type of configurability is referred to herein as "function enabling".

In an exemplary third type of configuration, a signal can be configured to be present or not. This type of configurability is referred to herein as "signal-enabling". **Figure 2b** represents a very simple logical interface, which can be used for cores with low performance requirements. A higher level of interface functionality and complexity may include the addition of a burst field (Mburst),

indicating that the addresses of subsequent commands are logically related. One embodiment of the burst encoding of the Mburst signal is shown in **Figure 3b.**

As indicated herein, an incrementing burst indicates a command sequence where the address increments by the number of bytes in the data word with every new command being issued in the burst. A non-incrementing burst is a burst sequence where the address remains unchanged between the commands in the burst. A core with burst configured in potentially allows much higher read and write throughput for transferring a large block of data. Again, this option can be optionally configured into the core interface if the core is used in a system that can take advantage of this feature.

The greater the configurability of the interface, the wider the usability of the core. One embodiment of an extended and highly configurable core interface is shown in **Figure 4**.

Some of the extensions illustrated by **Figure 4** include the ByteEnable Field (MByteEn) indicates which bytes in the MData Field are to be read or written; MError and SError that represent error signals; and MFlag and SFlag fields that are used for transferring out-of-band information between the core and the system. A traditional and well-known example of this kind of information is synchronization, where for example, the system is waiting for an out-of-band signal from the core before the system transmits any further requests.

One embodiment of a method of generating the optimal core is illustrated in **Figure 6**. At step 610, the core source code with at least one configurable interface parameter is provided. In one embodiment, for each interface configuration option, a parameter is defined, together with a range of allowable values. For example, for configuring the width the MData field of **Figure 4**, the parameter name MData_WIDTH is defined and the allowable values are 8,16,32 and 64. For signal-enabling the MBurst field, the parameter MBurst_ENABLE

can be defined with the allowable values of 0 and 1, where the value 0 indicates that it is not present and the value of indicates that it is.

In one embodiment, the core is implemented as configurable source code that makes use of these parameters or derived versions of these parameters. This source code can be in a variety of forms of e.g. commercially available hardware description languages (Verilog, VHDL) or software languages (C, perl, ...), or any combination of these or any other language.

At step 620, the configuration settings are provided. In one embodiment, the configuration settings are defined in a machine-readable form. In one embodiment, the configuration settings for a particular core are defined in a file. **Figure 5** shows an example of a configuration file describing a particular configuration of the interface described in **Figure 4.**

At step 625, the source code and configurations settings are combined, e.g., compiled, to generate the core with the configured interface. In one embodiment, a software program, referred to herein as the core compiler, process, step 625, the configurable source code representation of the core is combined with the data of the configuration to generate a core with the desired interface, step 630.

In one embodiment, the configuration settings can be entered manually by the user; alternatively the settings can be entered through a Graphical User Interface. **Figure 7** illustrates one embodiment of an example Graphical User Interface for configuring a set of options on a core with a configurable interface similar to the one described in **Figure 4.** These values, which are described by the text in the GUI window, are used by software, together with the configurable source code, to derive the core with the desired interface.

The invention has been described in conjunction with the preferred embodiment. It is evident that numerous alternatives, modifications, variations and uses will be apparent to those skilled in the art in light of the foregoing description.

CLAIMS

What is claimed is:

1. A computer core comprising at least one interface signal that is configurable such that the interface signal can be selectively present.

2. The computer core as set forth in claim 1, wherein at least one interface signal is further configured to support different levels of functionality.

3. The computer core as set forth in claim 2, wherein a signal width of at least one interface signal is configurable to support different signal widths.

4. A computer core comprising at least one interface signal that is configurable such that the interface signal can be configured to support different levels of functionality.

5. The computer core as set forth in claim 4, wherein a signal width of at least one interface signal is configurable to support different signal widths.

6. A computer core comprising at least one interface signal, a signal width of the at least one interface signal being configurable to support different signal widths.

7. A method for generating a computer core interface comprising:

providing configurable source code representative of the computer core and identifying parameters of the computer interface;

defining configuration parameters of the computer core interface; and

generating a computer core from the configurable source code comprising an interface comprising the identified parameters configurable in accordance with the defined configuration parameters.

8. The method as set forth in claim 7, wherein at least one of the configuration parameters are selected from the group comprising parameters that define whether the signal is present in the interface, define different levels of

functionality of the interface, and define a signal width of at lease one interface signal.

9. A method for generating a core with a configured interface comprising:

implementing the core as configurable source code utilizing at least one defined parameter of an interface of the core;

selecting at least one configuration option of the at least one defined parameter;

generating a core comprising a the at least one defined parameter of the core interface that operates in accordance with the selected interface comprising the selected at least one configuration option.

10. The method as set forth in claim 9, wherein selecting is performed through a graphical user interface.

11. The method as set forth in claim 9, wherein selecting is performed by deriving the configuration options from the configurations option of another core.

ABSTRACT

A core block with a highly configurable interface such that the interface of the core can be optimally configured for the system the core is integrated into. In one embodiment the method consists of defining a configurable interface with different configuration options, capturing the specific core configuration through manual entry or through the use of a Graphical User Interface, and providing for software that combines the source description of the core with the configuration data to generate the core with an optimally configured logic and circuit interface.

Figure 1a: Initial core (**Prior Art**)

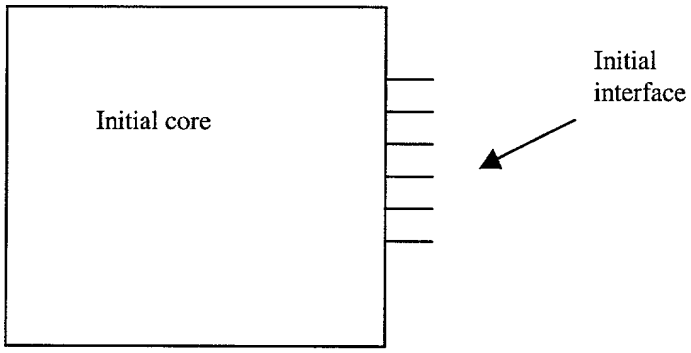


Figure 1b: Core with re-designed Interface (**Prior Art**)

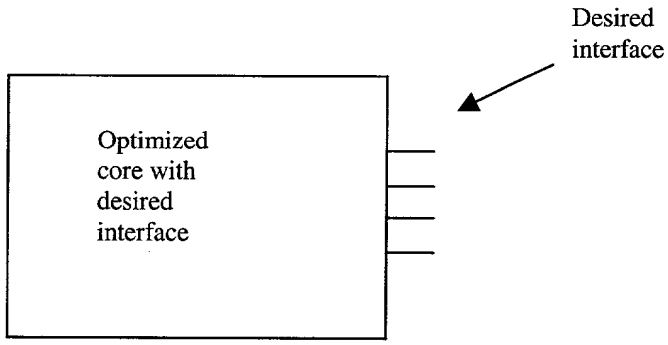


Figure 1c: Core of 1.a with external interface logic (**Prior Art**)

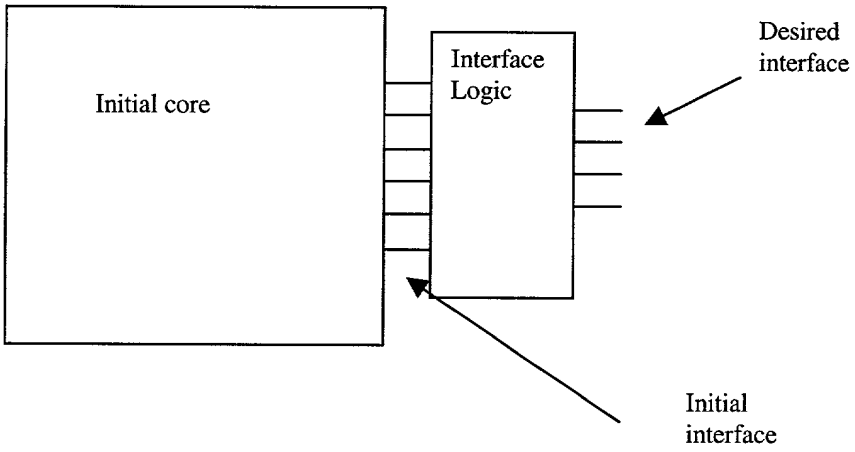


Figure 2a:

Name	Signal width	Function
Clk	1	Clock
MCmd	2	Command
MAddress	32	Address
Mdata	64	Write Data
SCmdAccept	1	Accept Command
SResp	2	Response
SData	64	Read Data

Figure 2b:

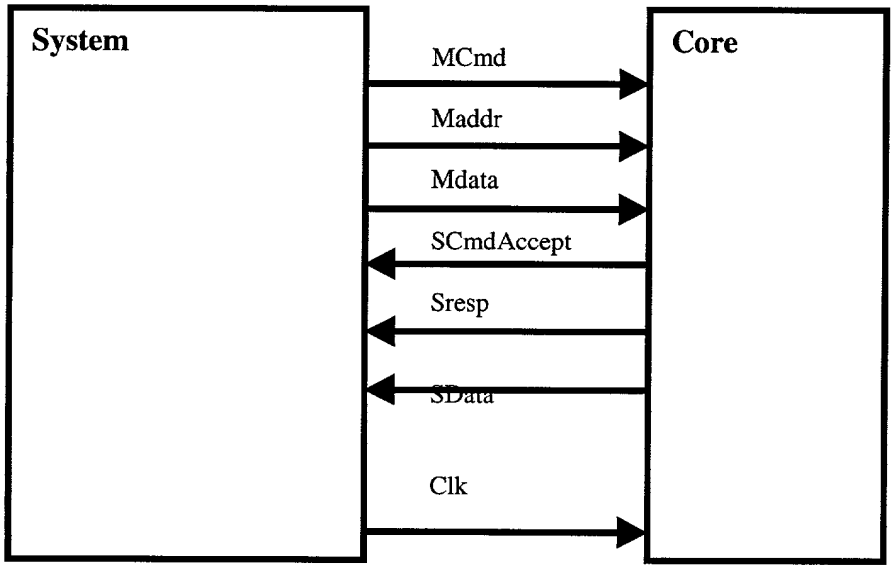


Figure 3a:

Command encoding	Function
00	Idle command
01	Read Command
10	Write Command
11	Exclusive Read Command

Figure 3b:

Burst encoding	Burst Function
000	Incrementing burst with burst length of 1
001	Incrementing burst with burst length of 2
010	Incrementing burst with burst length of 4
011	Incrementing burst with burst length of 8
100	Non-Incrementing burst

Burst encoding	Burst Function
000	Incrementing burst with burst length of 1
001	Incrementing burst with burst length of 2
010	Incrementing burst with burst length of 4
011	Incrementing burst with burst length of 8
100	Non-Incrementing burst

Figure 3c

Figure 4:

Signal Name	Width	Parametrization	Signal Enabling	Function
Clk	1	N	N	Clock
Reset	1	N	Y	Reset
MCmd	2	N	N	Request Command
MAddr	1-32	Y	N	Request Address
MData	8:16:32:64	Y	N	Request Write Data
MBurst	3	N	Y	Request Burst
MByteEn	1:2:4:8	Y	Y	Request Byte Enable
MDataValid	1	N	Y	Write Data Valid
SCmdAccept	1	N	N	Accept Command
SDataAccept	1	N	With MDataValid	Accept Write Data
SResp	2	N	N	Response
SData	8:16:32:64	Y	N	Read Response Data
MFlag	1:8	Y	Y	Master Out of Band signal
SFlag	1:8	Y	Y	Slave Out of Band Signal
MError	1	N	Y	Master Error
SError	1	N	Y	Slave Error

Figure 5:

MData_WIDTH	16
MAddr_WIDTH	32
MBurst_ENABLE	1
MByteEn_ENABLE	1
MByteEn_WIDTH	4
MDataValid_ENABLE	0
MFlag_ENABLE	1
MFlag_WIDTH	2
SFlag_ENABLE	0
MError_ENABLE	1
SError_ENABLE	0

Figure 6:

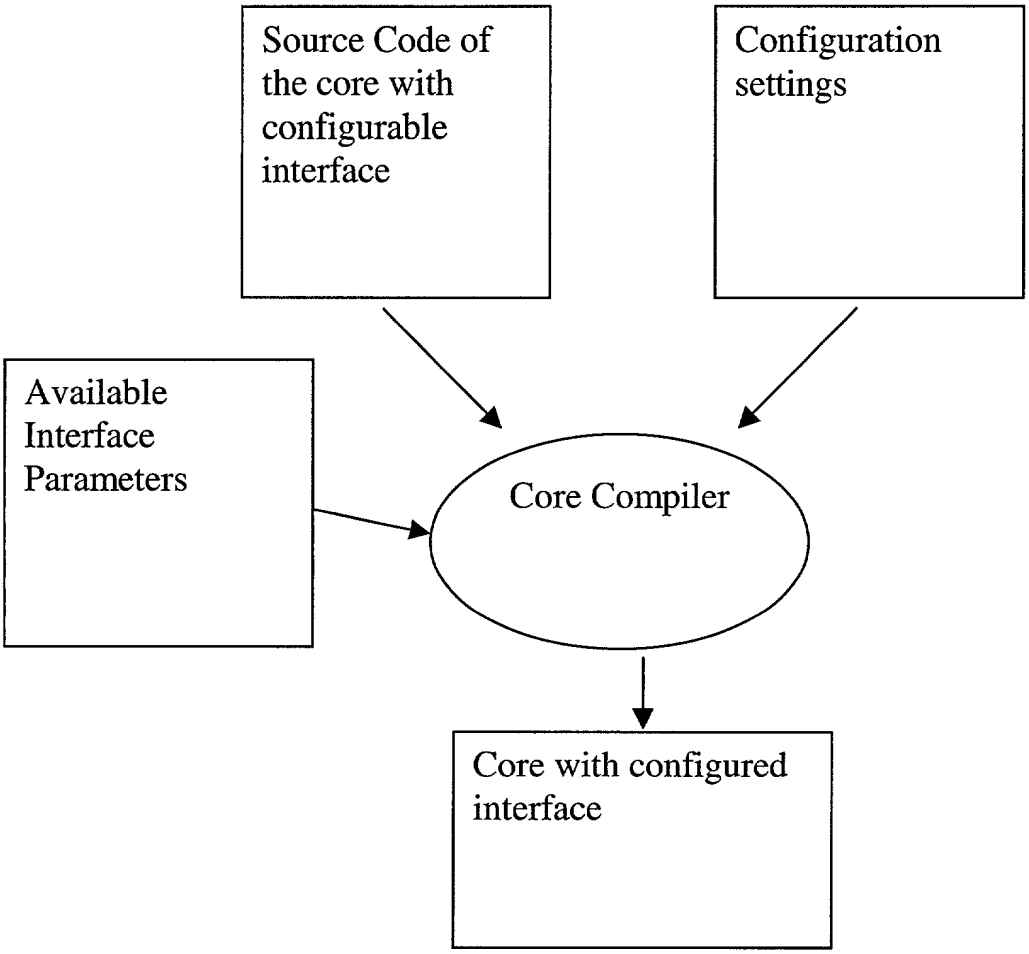
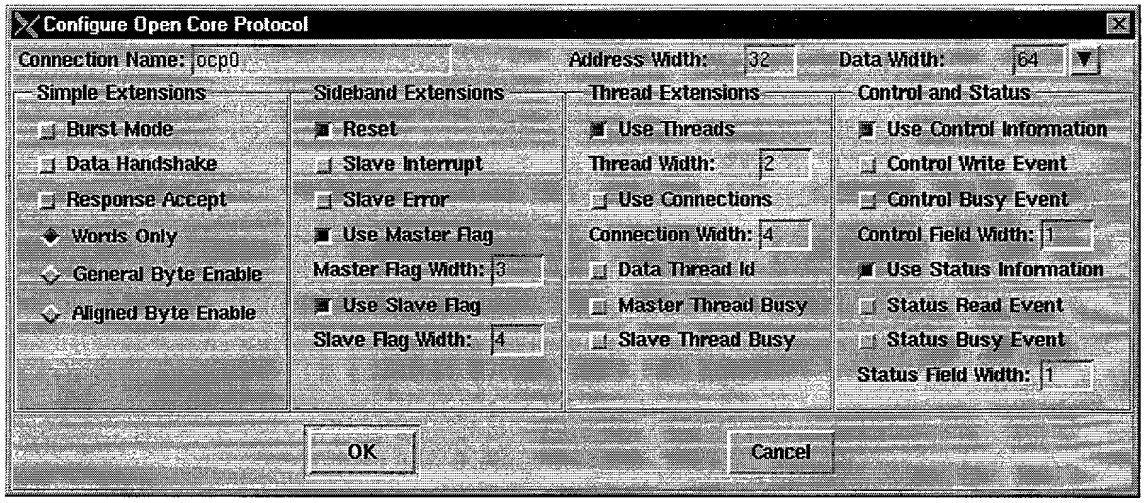

Source Code of the core with configurable interface
Configuration settings
Available Interface Parameters
Core Compiler
Core with configured interface

Figure 7:


Configure Open Core Protocol
Connection Name: ocp0
Address Width: 32
Data Width: 64
Simple Extensions
Burst Mode
Data Handshake
Response Accept
Words Only
General Byte Enable
Aligned Byte Enable
Sideband Extensions
Reset
Slave Interrupt
Slave Error
Use Master Flag
Master Flag Width: 3
Use Slave Flag
Slave Flag Width: 4
Thread Extensions
Use Threads
Thread Width: 2
Use Connections
Connection Width: 4
Data Thread Id
Master Thread Busy
Slave Thread Busy
Control and Status
Use Control Information
Control Write Event
Control Busy Event
Control Field Width: 1
Use Status Information
Status Read Event
Status Busy Event
Status Field Width: 1
OK
Cancel

Attorney's Docket No.: 02998.P011 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
Logic System with Configurable Interface

the specification of which

XXX is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

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(Name of Attorney or Agent)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature Jay L Tomlinson Date 8-7-00

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a *prima facie* case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.